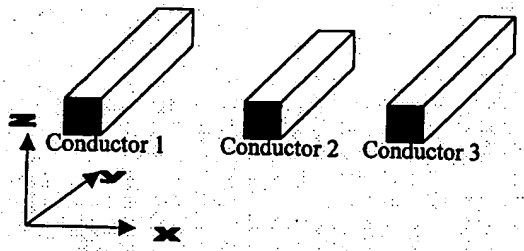
Figures



$$\text{Capacitance Matrix} = C = \begin{bmatrix} C_{11} C_{12} C_{13} \\ C_{21} C_{22} C_{23} \\ C_{31} C_{32} C_{33} \end{bmatrix}$$

coupling capacitances $= C_{ni}$, where n, i = conductor numbers

total capacitance $= C_{ntot} = \sum_{i=1}^{N} C_{ni}$, where N = the number of conductors

Figure 1a

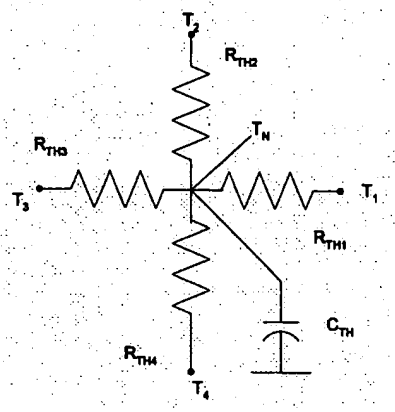


FIG. 1b

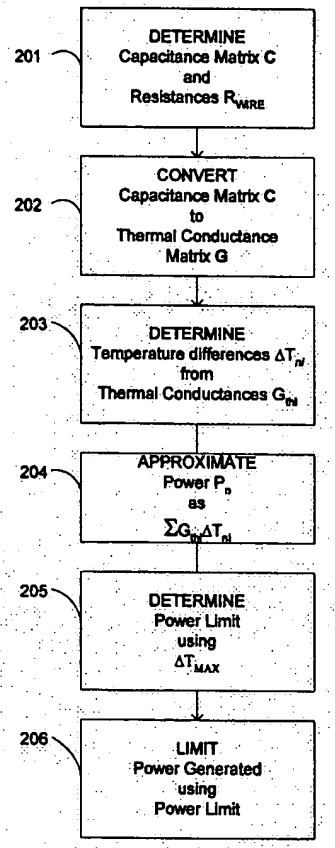

201
DETERMINE
Capacitance Matrix C
and
Resistances R_{WIRE}
202
CONVERT
Capacitance Matrix C
to
Thermal Conductance
Matrix G
203
DETERMINE
Temperature differences ΔT_{ni}
from
Thermal Conductances G_{ni}
204
APPROXIMATE
Power P_n
as
$\Sigma G_{ni} \Delta T_{ni}$
205
DETERMINE
Power Limit
using
ΔT_{MAX}
206
LIMIT
Power Generated
using
Power Limit

FIG. 2

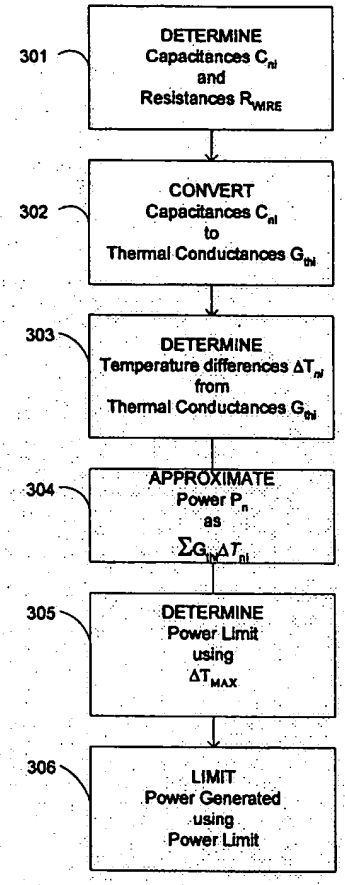

301
DETERMINE
Capacitances C_{ni}
and
Resistances R_{WIRE}
302
CONVERT
Capacitances C_{ni}
to
Thermal Conductances G_{thi}
303
DETERMINE
Temperature differences ΔT_{ni}
from
Thermal Conductances G_{thi}
304
APPROXIMATE
Power P_n
as
$\Sigma G_{thi} \Delta T_{ni}$
305
DETERMINE
Power Limit
using
ΔT_{MAX}
306
LIMIT
Power Generated
using
Power Limit

FIG. 3

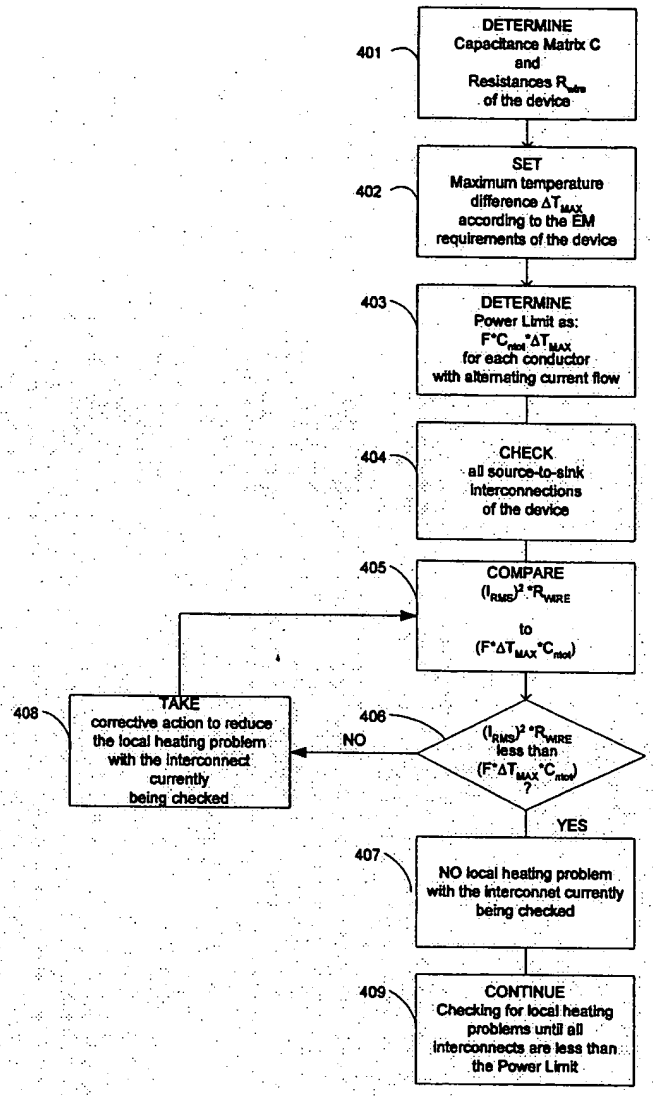

401
DETERMINE
Capacitance Matrix C
and
Resistances R_{wire}
of the device
402
SET
Maximum temperature
difference ΔT_{MAX}
according to the EM
requirements of the device
403
DETERMINE
Power Limit as:
$F^*C_{mat}{}^*\Delta T_{MAX}$
for each conductor
with alternating current flow
404
CHECK
all source-to-sink
interconnections
of the device
405
COMPARE
$(I_{RMS})^2{}^*R_{WIRE}$
to
$(F^*\Delta T_{MAX}{}^*C_{mat})$
406
$(I_{RMS})^2{}^*R_{WIRE}$
less than
$(F^*\Delta T_{MAX}{}^*C_{mat})$
?
NO
408
TAKE
corrective action to reduce
the local heating problem
with the interconnect
currently
being checked
YES
407
NO local heating problem
with the interconnet currently
being checked
409
CONTINUE
Checking for local heating
problems until all
interconnects are less than
the Power Limit

FIG. 4